REMARKS

The following remarks are made in response to the Final Office Action mailed November 24, 2004. Claims 37-48 were rejected. With this Response, no claims have been amended. Claims 37-48 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 37-46 under 35 U.S.C. § 102(b) as being anticipated by McLaughlin et al., U.S. Patent No. 5,202,822. Applicant submits that the McLaughlin et al. Patent does not teach or suggest the invention of independent claim 37.

The McLaughlin et al. Patent discloses a controller of a control system, which operates as a master, has a slave input/output processor (IOP) connected thereto which communicates with at least one device of a predetermined type, and a backup slave IOP connected thereto of the same type as the slave IOP, the slave IOP operating as a primary IOP to the device. A method for providing backup to the slave IOP by the backup slave IOP comprises the steps of loading the backup slave IOP with the same database as the slave IOP. The backup slave IOP eavesdrops on all communications from the controller to the slave IOP. When a write command is communicated to the slave IOP, the backup slave IOP taps the data from the bus and updates the database. If the command is not a write command, it ignores the communication. (Abstract).

The McLaughlin et al. Patent includes a process control system 10 including a plant control network 11, in which a process controller 20 is operatively connected to the plant control network 11. The process controller 20 interfaces analog input and output signals, and digital input and output signals to process control system 10 from a variety of field devices that include valves, pressure switches, pressure gauges, thermocouples, etc. (Column 3, lines 22-38). The process controller 20 includes a controller A 30 and a controller B 40 which effectively operate as a primary and secondary controller. (Column 3, lines 60-64). A database maintained by the primary controller is communicated to the secondary controller via link 13. (Column 4, lines 30-32; Fig. 2). A track unit is coupled to local bus 93 of

control unit 90 to implement the database transfer via link 13 to the other controller 30, 40 of the process controller 20. (Column 4, line 67 – column 5, line 3).

Controller A 30 interfaces to each I/O module 21 via a bus A 22, and controller B 40 interfaces to each I/O module 21 via a bus B 23. In addition, for redundancy purposes, controller A 30 is also connected to bus B 23 and controller B 40 is connected to bus A 22. (Column 4, lines 6-11). In I/O modules 21, signals on bus A 22 and bus B 23 are received by transceiver 201. Transceiver 201 communicates the signals to microcontroller 202. Microcontroller 202 communicates with EPROM 204 and RAM 205 through local bus 203. RAM 205 contains the information that forms the database for I/O module 21. (Column 5, lines 38-47; Fig. 4).

Synchronizing is a process whereby the same database is contained in both IOP(A) 21-A and IOP(B) 21-B. The information of the database of IOP(A) 21-A is requested by the controller 30 and then transferred to IOP(B) 21-B thereby causing the database of IOP(B) 21-B to be the same. (Column 8, lines 13-19). In normal operation, all write commands to IOP(A) 21-A from controller 30 are received by IOP(B) 21-B. IOP(B) 21-B eavesdrops on the communications. (Column 8, lines 28-31). IOP(B) 21-B eavesdrops on the communications by receiving all write commands from bus A 22.

Applicant submits that the McLaughlin et al. Patent does not teach or suggest the limitations of independent method claim 37 of synchronizing the memory device in the master control unit with the memory device in the slave control unit, the synchronizing including: generating, in the master control unit, values for the signal paths associated with the master memory device to transfer data to the master memory device; transferring a subset of the generated signal paths to the signal path associated with the slave memory device; and allowing the generated signals to perform the data transfer to the master memory device and the slave memory device.

The Examiner states in the Response to Arguments section that:

> in column 8, lines 28-33, McLaughlin et al. disclose that in normal operation, all transfers (i.e., writes) to the IOP(A) 21-A from controller are also received by IOP(B). IOP(B) eavesdrops on the communications since both IOP(A) and IOP(B) have a logical address of 1 in this example and the controller communicates to the IOPs by logical address. Further, in column 9, lines 60-65, McLaughlin et al. discloses that the read requests which were queued up by IOP(A) and not yet processed is known to the controller. The controller,

> then initiates to IOP(B) those read requests queued up at the time the failure of IOP(A) was detected. Thus, no communications (requests from other subsystems of system) go unanswered.

The synchronizing steps as recited in claim 37 are not disclosed in the McLaughlin et al. Patent. The eavesdropping cited by the Examiner is not the same as the synchronizing steps recited in claim 37. Claim 37 requires the master control unit *to generate, in the master control unit, values for the signal paths associated with the master memory device to transfer data to the master memory device.* Example embodiments of such a master control unit and master memory device which can implement these steps of claim 37 include the master control unit 212A and master memory device 234A illustrated in Figure 6 of the present application. Memory controller 224A of master control unit 212A ensures that the data in master memory device 234A and slave memory device 234B is consistent. (See specification, page 9, lines 20-21). The signal paths associated with master memory device 234A include memory bus 230A. The signal paths associated with slave memory device 234B include memory bus 230B. Bus switches 290, 292, and 294 are used to exchange data between the two memory buses 230A and 230B. (See specification, page 15, lines 7-21). Claim 37 requires master control unit 212A to generate values for signal paths 230A.

Claim 37 also requires *transferring a subset of the generated signal paths to signal paths associated with the slave memory device.* In one example implementation of the invention of claim 37, generated signal paths 230A associated with master memory device 234A are transferred to signal paths 230B associated with slave memory device 234B through bus switches 290, 292, and 294 of master control unit 212A and slave control unit 212 B.

In addition, claim 37 requires *allowing the generated signals to perform the data transfer to the master memory device and the slave memory device.* In one example implementation of the invention of claim 37, the signals generated in master control unit 212A perform the data transfer to master memory device 234A and slave memory device 234B through memory bus 230A and 230B, respectively.

In contrast, in the McLaughlin et al. Patent, IOP(A) 21-A and IOP(B) 21-B each individually receive signals for writing to their respective RAM memories 205 through bus A 22 or bus B 23 from controller A 30. There are no signals generated in slave IOP(A) 21-A that are transferred to backup slave IOP(B) 21-B. The signals provided to IOP(A) 21-A and IOP(B) 21-B are provided by controller A 30. Microcontroller 202 of each IOP 21 receives the signals from controller A 30 and can write data only to its own RAM 205 and not to the RAM of another IOP 21. In the method of claim 37, the slave control unit does not receive any signals from the data processor in the same manner as IOP(B) 21-B receives signals from controller A 30. In one example implementation of the invention of claim 37, slave memory device 234B is written by first memory controller 224A of master control unit 212A, not by second memory controller 224B of slave control unit 212B. The eavesdropping method described in the McLaughlin et al. Patent and cited by the Examiner provides a method for synchronization different than the method of synchronization recited in claim 37.

In summary, in the McLaughlin et al. Patent, synchronization is performed by controller A 30 communicating with microcontroller 202 of slave IOP(A) 21-A and microcontroller 202 of backup slave IOP(B) 21-B. Microcontroller 202 of slave IOP(A) 21-A writes RAM 205 of IOP(A) 21-A, and microcontroller 202 of backup slave IOP(B) 21-B writes RAM 205 of IOP(B) 21-B to synchronize the memories. IOP(A) 21-A does not communicate with IOP(B) 21-B. In contrast, in the method of claim 37, the master control unit communicates with the slave control unit to perform the data transfer to the slave memory device to synchronize the memories.

In view of the above, the McLaughlin et al. Patent does not teach or suggest the method of independent claim 37. Dependent claims 38-46 further define patentably distinct independent claim 37. Accordingly, dependent claims 38-46 are also believed to be allowable.

Therefore, Applicant respectfully requests that the rejections to claims 37-46 under 35 U.S.C. § 102 be withdrawn and that claims 37-46 be allowed.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claims 47 and 48 under 35 U.S.C. § 103(a) as being unpatentable over the McLaughlin et al. Patent as applied to claim 37, and further in view of Kern et al, U.S. Patent No. 5,734,818.

Dependent claims 47 and 48 further define patentably distinct independent claim 37. Accordingly, dependent claims 47 and 48 are also believed to be allowable.

Therefore, Applicant respectfully requests that the rejections to claims 47 and 48 under 35 U.S.C. § 103 be withdrawn and that claims 47 and 48 be allowed.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 37-48 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 37-48 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either David A. Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854 or Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Hewlett-Packard Company
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Respectfully submitted,

Jong Chan,

By his attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-2003
Facsimile: (612) 573-2005

Date: 1-24-05
PGB: kle

Patrick G. Billig
Reg. No. 38,080

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 24 day of January, 2005.

By
Name: Patrick G. Billig